



Doc. Number:

☐ Tentative Specification
□ Preliminary Specification
Approval Specification

MODEL NO.: N140BGE SUFFIX: -L31(Rev C1)

Customer: HP	
APPROVED BY	SIGNATURE
Name / Title Note	
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方健穎	/ · / · // · ·
	陳郁甫
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REVISION HISTORY

Version	Date	Page	Description
3.0	Dec 27, 2010	All	Spec Ver.3.0 was first issued for HP.
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1. GENERAL DESCRIPTION

1.1 OVERVIEW

N140BGE-L31 is a 14.0" (14.0" diagonal) TFT Liquid Crystal Display module with LED Backlight unit and 40 pins LVDS interface. This module supports 1366 x 768 HD mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction.

1.2 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Screen Size	14.0" diagonal		
Driver Element	a-si TFT active matrix	4	-
Pixel Number	1366 x R.G.B. x 768	pixel	-
Pixel Pitch	0.2265 (H) x 0.2265 (V)	mm	-
Pixel Arrangement	RGB vertical stripe		-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hard coating (3H), Anti-Glare	-	-
Luminance, White	200	Cd/m2	
Power Consumption	Total 4 W (Max.) @ cell 1 W (Max.), BL 3 W (Max.)		(1)

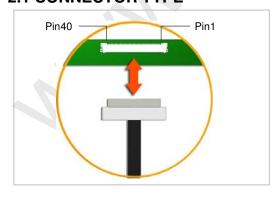
Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, fv = 60 Hz, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 $^{\circ}\text{C}$, whereas mosaic pattern is displayed.

2. MECHANICAL SPECIFICATIONS

	Item	Min.	Тур.	Max.	Unit	Note
	Horizontal (H)	319.9	320.4	320.9	mm	
Module Size	Vertical (V)	198.1	198.6	199.1	mm	(1)
	Thickness (T)	-	-	3.6	mm	
Active Area	Horizontal	-	309.399	-	mm	
Active Area	Vertical	-	173.952	-	mm	
V	Veight	-	310	320	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2.1 CONNECTOR TYPE



Please refer Appendix Outline Drawing for detail design.

Connector Part No.: IPEX-20455-040E-12 or equivalent

User's connector Part No: IPEX-20453-040T-01 or equivalent

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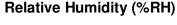
3. ABSOLUTE MAXIMUM RATINGS

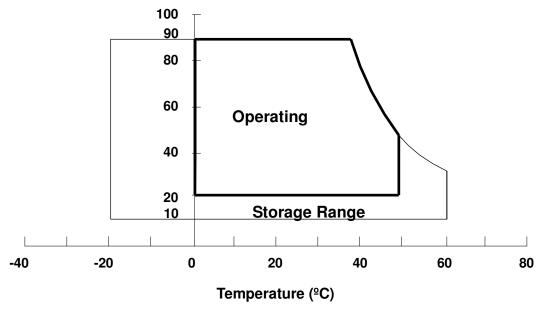
3.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Va	lue	Unit	Note	
nem	Symbol	Min.	Max.	Offic		
Storage Temperature	T _{ST}	-20	+60	ºC	(1)	
Operating Ambient Temperature	T _{OP}	0	+50	ºC	(1), (2)	

- (a) 90 %RH Max. (Ta $<= 40 \, {}^{\circ}\text{C}$). Note (1)
 - (b) Wet-bulb temperature should be 39 °C Max. (Ta > 40 °C).
 - (c) No condensation.

The temperature of panel surface should be 0 °C min. and 60 °C max. Note (2)





3.2 ELECTRICAL ABSOLUTE RATINGS

3.2.1 TFT LCD MODULE

Item	Symbol	Va	lue	Unit	Note	
Item	Cymbol	Min.	Max.	Offic	14010	
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)	
Logic Input Voltage	V_{IN}	-0.3	VCCS+0.3	V	(1)	
Converter Input Voltage	LED_VCCS	-0.3	25.0	V	(1)	
Converter Control Signal Voltage	LED_PWM,	-0.3	4.0	V	(1)	
Converter Control Signal Voltage	LED_EN	-0.3	4.0	V	(1)	

Note (1) Stresses beyond those listed in above "ELECTRICAL ABSOLUTE RATINGS" may cause permanent damage to the device. Normal operation should be restricted to the conditions described in "ELECTRICAL CHARACTERISTICS".

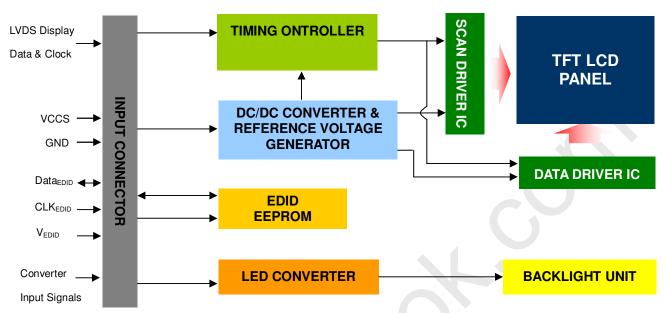
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4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

PIN ASS	SIGNMENT		
Pin	Symbol	Description	Remark
1	NC	No Connection (Reserve)	
2	VCCS	Power Supply (3.3V typ.)	
3	VCCS	Power Supply (3.3V typ.)	
4	VEDID	DDC 3.3V power	
5	NC	No Connection (Reserved for CMI test)	
6	CLKEDID	DDC clock	
7	DATAEDID	DDC data	
8	Rxin0-	LVDS differential data input	R0-R5, G0
9	Rxin0+	LVDS differential data input	nu-no, Gu
10	VSS	Ground	
11	Rxin1-	LVDS differential data input	G1~G5, B0, B1
12	Rxin1+	LVDS differential data input	G1~G5, B0, B1
13	VSS	Ground	
14	Rxin2-	LVDS Differential Data Input	B2-B5,HS,VS, DE
15	Rxin2+	LVDS Differential Data Input	B2-B3,113, V3, DE
16	VSS	Ground	
17	RxCLK-	LVDS differential clock input	LVDS CLK
18	RxCLK+	LVDS differential clock input	LVD3 CLR
19	VSS	Ground	
20	NC	No Connection (Reserve)	
21	NC	No Connection (Reserve)	
22	VSS	Ground	
23	NC	No Connection (Reserve)	

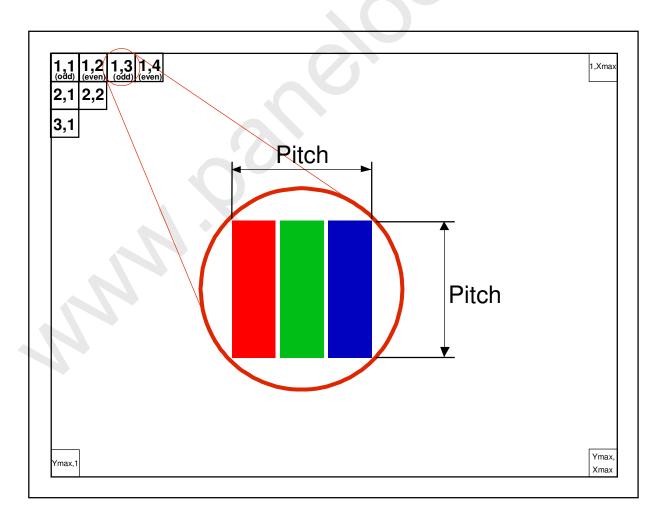
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24	NC	No Connection (Reserve)	
25	VSS	Ground	
26	NC	No Connection (Reserve)	
27	NC	No Connection (Reserve)	
28	VSS	Ground	
29	NC	No Connection (Reserve)	
30	NC	No Connection (Reserve)	
31	LED_GND	LED Ground	
32	LED_GND	LED Ground	
33	LED_GND	LED Ground	
34	NC	No Connection (Reserve)	
35	LED_PWM	PWM Control Signal of LED Converter	
36	LED_EN	Enable Control Signal of LED Converter	
37	NC	No Connection (Reserve)	
38	LED_VCCS	LED Power Supply	
39	LED_VCCS	LED Power Supply	
40	LED_VCCS	LED Power Supply	

Note (1) The first pixel is odd as shown in the following figure.



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4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

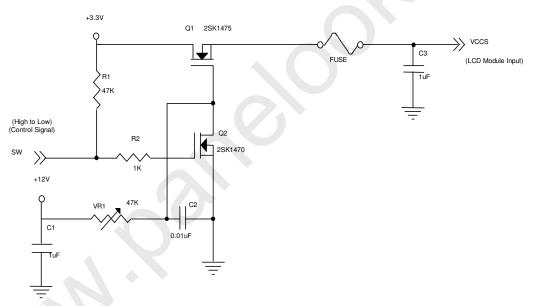
Parameter		Symbol	Value			Unit	Note
		Symbol	Min.	Тур.	Max.	Offic	Note
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)-
Ripple Voltage		V_{RP}	-	50	-	mV	(1)-
Inrush Current		I _{RUSH}	-	-	1.5	Α	(1),(2)
Power Supply Current	Mosaic Mosaic		-	250	280	mA	(3)a
Black		lcc	-	270	300	mA	(3)b
Power per EBL WG		P _{EBL}	-	1.52	-	W	(4)

Note (1) The ambient temperature is Ta = 25 ± 2 $^{\circ}$ C.

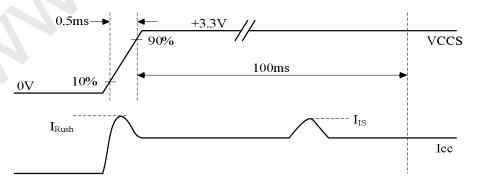
Note (2) I_{RUSH}: the maximum current when VCCS is rising

 $\ensuremath{I_{\text{IS}}}\xspace$ the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.



VCCS rising time is 0.5ms



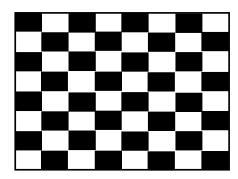
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Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 $^{\circ}$ C, DC Current and f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern



b. Black Pattern



Active Area
Note (4) The specified power are the sum of LCD panel electronics input power and the converter input power. Test conditions are as follows.

- (a) VCCS = 3.3 V, Ta = 25 \pm 2 $^{\varrho}C,\,f_{\nu}$ = 60 Hz,
- (b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.
- (c) Luminance: 60 nits.

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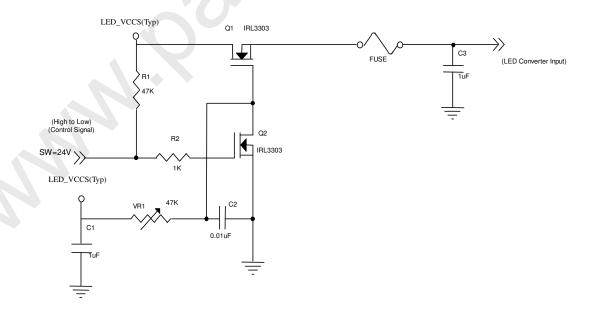
4.3.2 LED CONVERTER SPECIFICATION

Doros	motor	Cumbal		Value		Unit	Note	
Parar	neter	Symbol	Min.	Тур.	Max.	Unit		
Converter Input pow	LED_Vccs	6.0	12.0	21.0	V			
Converter Inrush Cu	Converter Inrush Current			-	1.5	Α	(1)	
EN Control Level	Backlight On		3.0	-	3.6	V		
EN CONTION Level	Backlight Off		0	-	0.5	V		
PWM Control Level	PWM High Level		3.0	-	3.6	V		
F WW Control Level	PWM Low Level		0	-	0.5	V		
PWM Control Duty F	Ratio		5	-	100	%	(2)	
PWM Control F Voltage	VPWM_pp	-	-	100	mV			
PWM Control Frequ	PWM Control Frequency			-	2K	Hz	(3)	
LED Power Current	ILED	181	213	247	mA	(4)		

Note (1) ILED_{RUSH}: the maximum current when LED_VCCS is rising,

ILED_{IS}: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 °C, f_{PWM} = 200 Hz, Duty=100%.

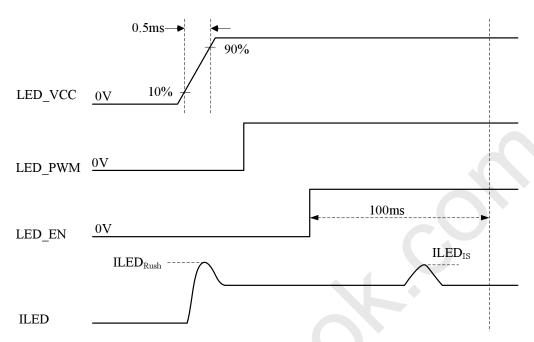


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VLED rising time is 0.5ms



- Note (2) If the PWM control duty ratio is less than 5%, there is some possibility that backlight flash can be found. And it is also difficult to control the brightness linearity.
- Note (3) If PWM control frequency is applied in the range less than 1KHz, the "waterfall" phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency
$${\sf f_{PWM}}$$
 should be in the range
$$(N+0.33)*f \le {\sf f_{PWM}} \le (N+0.66)*f$$

$$N: {\sf Integer} \ \ (N\ge 3)$$

$$f: {\sf Frame \ rate}$$

Note (4) The specified LED power supply current is under the conditions at "LED_VCCS = Typ.", Ta = 25 \pm 2 $^{\circ}$ C, f_{PWM} = 200 Hz, Duty=100%.



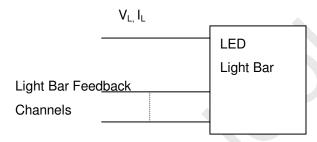


4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 ^oC

Davamatav	Cymahal		Value	Lloit	Note		
Parameter	Symbol	Min.	Тур.	Max.	Unit	Note	
LED Light Bar Power Supply Voltage	VL	27	28.8	30.6	V	(1)(2)(Duty1009()	
LED Light Bar Power Supply Current	lL	76	80	84	mA	(1)(2)(Duty100%)	
Power Consumption	PL	2.052	2.304	2.57	W	(3)	
LED Life Time	L_BL	12000	-	-	Hrs	(4)	

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ± 2 °C and I_L = 20 mA(Per EA) until the brightness becomes $\leq 50\%$ of its original value.

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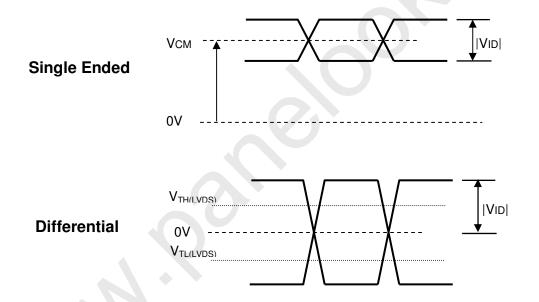


4.4 LVDS INPUT SIGNAL TIMING SPECIFICATIONS

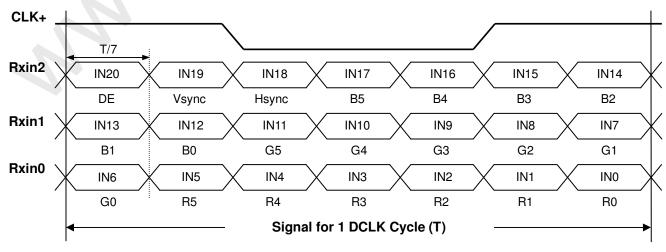
4.4.1 LVDS DC SPECIFICATIONS

Parameter	Symbol		Value		Unit	Note
	,	Min.	Min. Typ.			
LVDS Differential Input High Threshold	$V_{TH(LVDS)}$	-	-	+100	mV	(1), V _{CM} =1.2V
LVDS Differential Input Low Threshold	$V_{TL(LVDS)}$	-100	-	-	mV	(1) V _{CM} =1.2V
LVDS Common Mode Voltage	V_{CM}	1.125	-	1.375	V	(1)
LVDS Differential Input Voltage	$ V_{ID} $	100	-	600	mV	(1)
LVDS Terminating Resistor	R_T		100		Ohm	-

Note (1) The parameters of LVDS signals are defined as the following figures.



4.4.2 LVDS DATA FORMAT



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4.4.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

	<u> </u>								[Data		al							
	Color			Re						Gre					Blue				
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	В3	B2	B1	B0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Basic	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Colors	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Scale	:	:	:	:	:	:	:	:	:	:	:			:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:			:	:	:	:	:	:	:
Red	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Gray	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Scale	:	:	:	:	:	:		;	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:				:	:	:	:	:	:	:	:	:	:	:
Green	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Gray	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Scale	:			·	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	;	;	:	:	;
Blue	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1]	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

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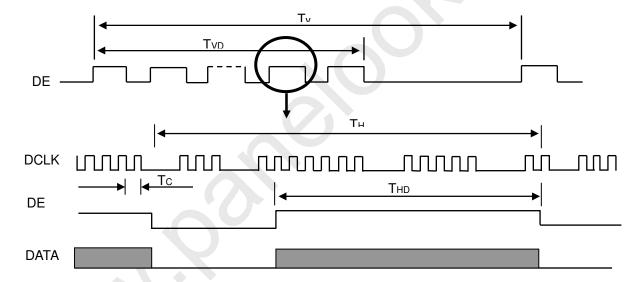
4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Тур.	Max.	Unit	Note
DCLK	Frequency	1/Tc	45	71	85	MHz	-
	Vertical Total Time	TV	780	790	900	TH	-
	Vertical Active Display Period	TVD	768	768	768	TH	-
DE	Vertical Active Blanking Period	TVB	TV-TVD	22	TV-TVD	TH	-
DE	Horizontal Total Time	TH	1408	1498	1800	Тс	-
	Horizontal Active Display Period	THD	1366	1366	1366	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	132	TH-THD	Tc	-

Note (1) Because this module is operated by DE only mode, Hsync and Vsync are ignored.

INPUT SIGNAL TIMING DIAGRAM



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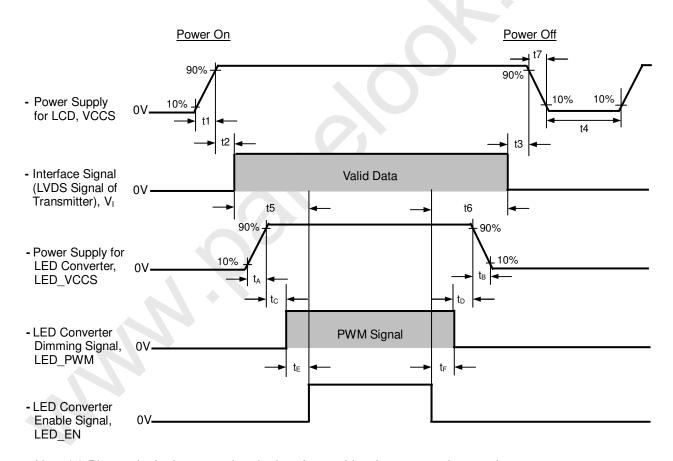
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PRODUCT SPECIFICATION

4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.

Cumbal		Value		Lloit	Note
Symbol	Min.	Тур.	Max.	Unit	Note
t1	0.5	-	10	ms	
t2	0	-	50	ms	
t3	0	-	50	ms	
t4	500	-	-	ms	
t5	200	-	-	ms	
t6	200	-	-	ms	
t7	0.5	-	10	ms	
t _A	0.5	-	10	ms	
t _B	0		10	ms	
t _C	10	-	-	ms	
t _D	10	-	-	ms	
t _E	10	-	-	ms	
t _F	10	-	-	ms	



- Note (1) Please don't plug or unplug the interface cable when system is turned on.
- Note (2) Please avoid floating state of the interface signal during signal invalid period.
- Note (3) It is recommended that the backlight power must be turned on after the power supply for LCD and the interface signal is valid.

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PRODUCT SPECIFICATION

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

Item	Symbol	Value	Unit			
Ambient Temperature	Ta	25±2	°C			
Ambient Humidity	На	50±10	%RH			
Supply Voltage	V_{CC}	3.3	V			
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"					
LED Light Bar Input Current	lμ	80	mA			

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Iter	n	Symbol	Condition	Min.	Тур.	Max.	Unit	Note
Contrast Ratio		CR		300	500	_	-	(2), (5) (7)
Doonanaa Tima		T_R		-	3	8	ms	(2) (7)
Response Time		T _F		-	8	13	ms	(3),(7)
Average Lumina	verage Luminance of White			170	200	-	cd/m ²	(4), (6),(7)
	Rod	Rx	$\theta_x=0^\circ, \theta_Y=0^\circ$		0.586		-	
	1100	Ry	Viewing Normal Angle		0.355		-	
	Groon	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	-					
Color	Green	Gy		Тур –	0.563	Typ +	-	(1),(7)
Chromaticity	Dluc	Bx			0.160	0.03	-	
	Blue	Ву			0.144		-	
	\\/bita	Wx			0.313		-	i
	vviiite	Wy			0.329		- ms ms ms cd/m² Deg	
	Horizontal	θ_{x} +		40	45			
Viewine Anale	ПОПИОПІАІ	θ_{x} -	OD: 10	40	45	-	Dag	(1),(5),
Viewing Angle	\/autiaal	θ_{Y} +	CR≥10	15	20	-	Deg.	(7)
	Vertical	θ _Y -		40	45	-		
NAME TO A MARKET OF THE PARTY O		δW_{5p}	$\theta_x=0^\circ, \ \theta_Y=0^\circ$		1.25	1.42	-	(5),(6),
White Variation		δW _{13p}	$\theta_x=0^\circ$, $\theta_Y=0^\circ$		1.33	1.66		(7)

Note (1) Definition of Viewing Angle (θx , θy)

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Normal $\theta x = \theta y = 0^{\circ}$ $\theta y = \theta y = 0^{\circ}$ $\theta x = \theta y = 0^{\circ}$ $\theta y = \theta y = 0^{\circ}$ $\theta x = \theta y = 0^{\circ}$ $\theta y = \theta y = 0^{\circ}$ $\theta x = \theta y = 0^{\circ}$ $\theta y = \theta y = 0^{\circ}$ $\theta x = \theta y = 0^{\circ}$



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

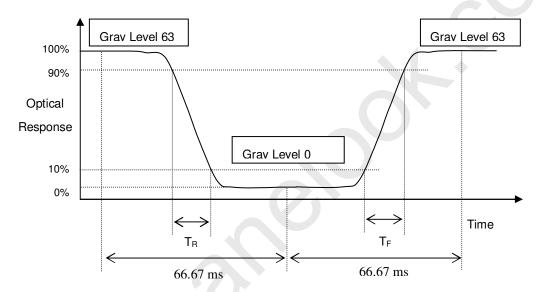
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR(1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R , T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

Measure the luminance of White at 5 points

$$L_{AVE} = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$$

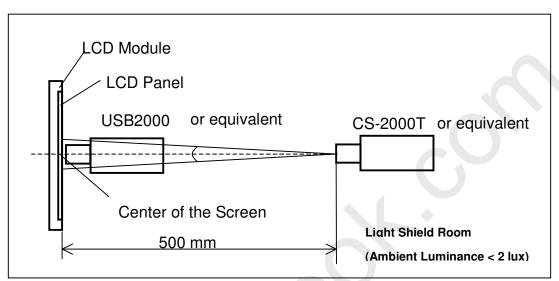
L(x) is corresponding to the luminance of the point X at Figure in Note (6)





Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

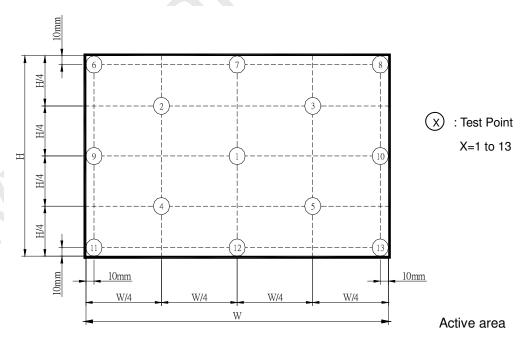


Note (6) Definition of White Variation (δW):

Measure the luminance of White at 5 points

$$\delta W_{5p} = \{Maximum [L (1)~L (5)] / Minimum [L (1)~L (5)]\}$$

$$\delta W_{13p}$$
 = Maximum [L(1) \sim L(13)] / Minimum [L(1) \sim L(13)]



Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

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6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60ºC, 240 hours	
Low Temperature Storage Test	-20ºC, 240 hours	
Thermal Shock Storage Test	-20°C, 0.5hour ←→60°C, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	50°C, 240 hours	(1) (2)
Low Temperature Operation Test	0ºC, 240 hours	() ()
High Temperature & High Humidity Operation Test	50℃, 80% RH, 240 hours	
ESD Test (Operation)	150pF, 330 Ω, 1sec/cycle Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±15KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave,1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

- Note (1) criteria: Normal display image with no obvious non-uniformity and no line defect.
- Note (2) Evaluation should be tested after storage at room temperature for more than two hour
- Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

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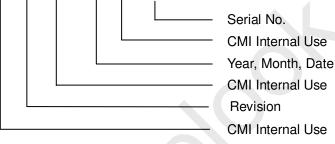
7. PACKING

7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: N140BGE L31
- (b) Revision: Rev. XX, for example: C1, C2 ...etc.
- (c) Serial ID: XXXXXXXXYMDXNNN



- (d) Production Location: MADE IN XXXX.
- (e) UL/CB logo: "XXXX" especially stands for panel manufactured by CMI Ningbo satisfying UL/CB requirement. "LEOO" "CANO" is the CMI's UL factory code for Ningbo factory.

Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2001~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I, O and U

- (b) Revision Code: cover all the change
- (c) Serial No.: Manufacturing sequence of product
- (d) Product Line: 1 -> Line1, 2 -> Line 2, ...etc.

CT Label

S/N	CT: CBQYFXX5CXXXXX
СТ:	Title
С	LCD Display Module
BQYF	Assembly Code
XX	Revision
5C	Supplier /Site of MFG
XX	Week/Year of MFG
XXX	Serial number. From 000000 to 999999

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Box Dimensions: 435(L)*350(W)*320(H)





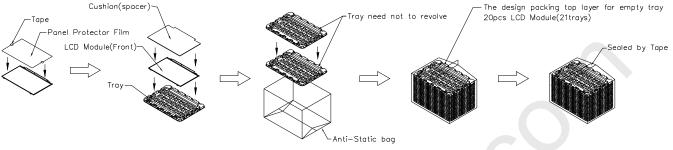
PRODUCT SPECIFICATION

7.2 CARTON

Weight: Approx. 9.6kg(20 module .per. 1 box)

Cushion(spacer)

Tray need not to revolve



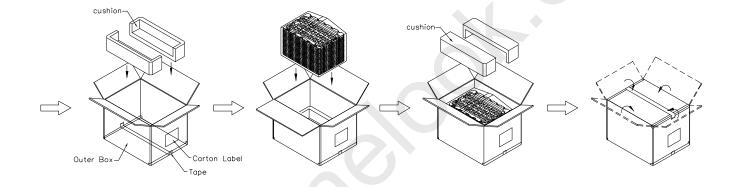


Figure. 7-2 Packing method

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7.3 PALLET

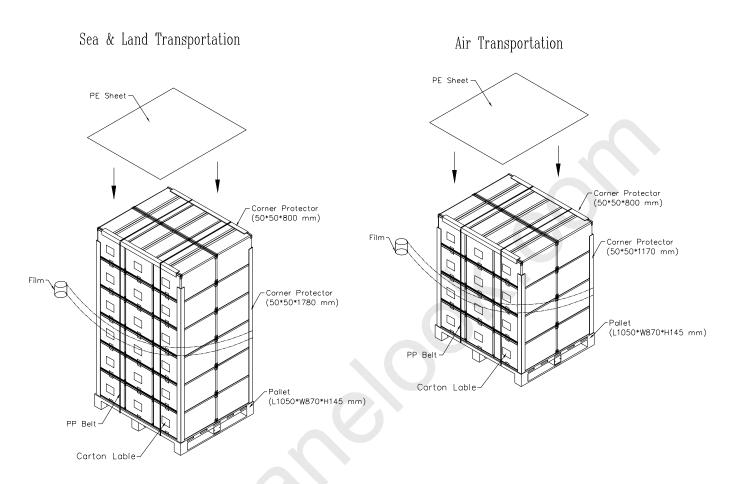


Figure. 7-3 Packing method

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8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

- (1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.
- (2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
- (3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
- (5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
- (6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.
- (9) Do not disassemble the module.
- (10) Do not pull or fold the LED wire.
- (11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

- (1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
- (3) It may reduce the display quality if the ambient temperature is lower than 10 °C. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

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- (1) Do not pull the I/F connector in or out while the module is operating.
- (2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMIS LSI chips from damage during latch-up.
- (3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

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Appendix. EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

VESA	Plug & I	Display and FPDI standards.		
Byte #	Byte #	Field Name and Comments	Value	Value
(decimal)			(hex)	(binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name ("CMO")	0D	00001101
9	9	EISA ID manufacturer name (Compressed ASCII)	AF	10101111
10	0A	ID product code (N140BGE-L31)	67	01100111
11	0B	ID product code (hex LSB first; N140BGE-L31)	14	00010100
12	0C	ID S/N (fixed "0")	00	00000000
13	0D	ID S/N (fixed "0")	00	00000000
14	0E	ID S/N (fixed "0")	00	00000000
15	0F	ID S/N (fixed "0")	00	00000000
16	10	Week of manufacture (fixed week code)	26	00100110
17	11	Year of manufacture (fixed year code)	14	00010100
18	12	EDID structure version # ("1")	01	0000001
19	13	EDID revision # ("4")	04	00000100
20	14	Video I/P definition ("digital")	90	10010000
21	15	Active area horizontal 31cm	1F	00011111
22	16	Active area vertical 18cm	12	00010010
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("Active off, RGB Color")	0A	00001010
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	05	00000101
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	35	00110101
27	1B	Rx=0.586	96	10010110
28	1C	Ry=0.355	5B	01011011
29	1D	Gx=0.317	51	01010001
30	1E	Gy=0.563	90	10010000
31	1F	Bx=0.16	29	00101001
32	20	By=0.144	24	00100100
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer's reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 1 Standard timing ID # 2	01	00000001
41		Standard timing ID # 2	01	00000001
71	29	Dianuaru liitiity ID # 2	υı	30000001

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42 2A Standard timing ID # 3 01 00000001 43 2B Standard timing ID # 3 01 00000001 44 2C Standard timing ID # 4 01 00000001 45 2D Standard timing ID # 5 01 00000001 47 2F Standard timing ID # 5 01 00000001 48 30 Standard timing ID # 6 01 00000001 50 31 Standard timing ID # 7 01 00000001 51 32 Standard timing ID # 8 01 00000001 52 34 Standard timing ID # 8 01 00000001 53 35 Standard timing ID # 8 01 00000001 54 36 Standard timing ID # 8 01 00000001 55 37 # 1 Pixel clock (Nox LSB first) 18 00000001 54 36 Standard timing ID # 8 01 00000001 55 37 # 1 Pixel clock (Nox LSB first) 18 001 <td< th=""><th>T</th><th>1</th><th>1</th><th>1</th><th>Γ</th></td<>	T	1	1	1	Γ
44 2C Standard timing ID # 4 01 00000001 45 2D Standard timing ID # 5 01 00000001 46 2E Standard timing ID # 5 01 00000001 47 2F Standard timing ID # 5 01 00000001 48 30 Standard timing ID # 6 01 00000001 59 32 Standard timing ID # 6 01 00000001 50 32 Standard timing ID # 7 01 00000001 51 33 Standard timing ID # 7 01 00000001 52 34 Standard timing ID # 8 01 00000001 53 35 Standard timing ID # 8 01 00000001 54 36 Standard timing ID # 8 01 00000001 55 37 # 1 Pixel clock ("69.3MHz", According to VESA CVT Rev1.1) 55 37 # 1 Pixel clock (hex LSB first) 1B 00011011 56 38 # 1 H active ("1366") 56 01010110 57 39 # 1 H blank ("100") 50 01010000 58 3A # 1 H active ("1486") 50 010101000 59 3B # 1 V active ("768") 00 00000001 60 3C # 1 V blank ("20") 14 00010101 61 3D # 1 V active ("V blank ("768 :20") 30 0110000 62 3E # 1 H sync pulse width ("32") 14 0001010 63 3F # 1 H sync pulse width ("32") 20 00100000 64 40 # 1 V sync offset : V sync pulse width ("1 : 4") 14 0001010 65 41 H l mage size ("174 mm') 35 0110110 66 42 # 1 H image size ("174 mm') 35 0110100 67 43 # 1 V sync offset : V sync pulse width ("1 : 4") 41 H image size ("174 mm') AE 10101110 68 44 # 1 H image size ("174 mm') AE 10101110 69 45 # 1 H boarder ("0") 00 00000000 70 46 # 1 V blank ("20") 10 00 000000000000000000000000000000	42	2A	Standard timing ID # 3	01	00000001
45 2D Standard timing ID # 4 46 2E Standard timing ID # 5 47 2F Standard timing ID # 5 48 30 Standard timing ID # 6 49 31 Standard timing ID # 6 50 32 Standard timing ID # 7 51 33 Standard timing ID # 7 52 34 Standard timing ID # 8 53 35 Standard timing ID # 8 54 Detailed timing ID # 8 55 37 # 1 Pixel clock (nex LSB first) 56 38 # 1 H active ("1366") 57 39 # 1 H blank ("100") 58 3A # 1 H active ("1366") 59 3B # 1 V active ("768") 60 3C # 1 V sync offset: V sync offset: V sync width 61 40 # 1 H image size ("309 mm") 63 47 # 1 Pixel clock (now LSB first) 64 48 # 1 H image size ("174 mm") 65 47 # 1 H image size ("309 mm") 66 47 # 2 V active ("1366") 77 40 # 2 V active ("1366") 78 48 # 1 H blank ("100") 79 4F # 2 V active ("1366") 70 40 00000000 71 40 # 2 V square ("1000000000000000000000000000000000000	43	2B	Standard timing ID # 3	01	0000001
46 2E Standard timing ID #5 01 00000001 47 2F Standard timing ID #5 01 00000001 48 30 Standard timing ID #6 01 00000001 49 31 Standard timing ID #6 01 00000001 50 32 Standard timing ID #7 01 00000001 51 33 Standard timing ID #7 01 00000001 52 34 Standard timing ID #7 01 00000001 53 35 Standard timing ID #8 01 00000001 54 36 VESA CVT Rev1.1) 12 10111100 55 37 #1 Pixel clock (hex LSB first) 12 10111100 55 37 #1 Pixel clock (hex LSB first) 18 00011011 56 38 #1 H active ("1366") 56 010101101 57 39 #1 H blank ("100") 64 10000100 58 3A #1 H active ("768") 50 01010000 59 3B #1 V Standard ("20") 14 0001101 61 3D #1 V Sandard ("368") 30 01110000 62 3E #1 H sync offset ("48") 30 01110000 63 3F #1 H sync offset ("48") 30 01110000 64 40 #1 V sync offset ("48") 30 00110000 65 41 ("48", 32 : 1 : 4") 41 H inage size ("309 mm") AE 1011110 66 42 #1 H inage size : V image size ("309 : 174") 10 00000000 70 46 #1 V Boarder ("0") 00000000 71 4D VESA CVT Rev1.1) 10 00000000 72 4A #1 Pixel clock (hex LSB first) 10 00000000 73 49 #1 Pixel clock ("68") 30 00110000 74 4A #1 H inage size : V image size ("309 : 174") 10 00000000 75 4B #2 H blank ("100") 50 00000000 76 4C #2 #1 H inage size : V image size ("309 : 174") 10 00000000 77 4D VESA CVT Rev1.1) 12 00000000 78 4P #1 Pixel clock ("46 .21MHz", According to VESA CVT Rev1.1) 11 1101100 78 4P #1 Pixel clock (hex LSB first) 10 00000000 79 4F #1 Pixel clock (hex LSB first) 10 00000000 70 4F #1 H sync offset ("48") 10 000000000 71 4D VESA CVT Rev1.1) 10 00000000 72 4D VESA CVT Rev1.1) 11 1101001 73 49 #1 Pixel clock (hex LSB first) 12 00000000 74 4A #2 H active ("1366") 56 00000000 75 4B #2 H active ("1366") 50 00000000 76 4F #2 H active ("1366") 50 00000000 77 4D WESA CVT Rev1.1) 11 11010001 78 4E #2 V active : V blank ("768 :20") 30 00110001 79 4F #2 V active : V blank ("1366 : 100") 50 00000000 80 50 #2 H sync offset ("48") 30 00110001 81 51 #2 H sync offset : V sync pulse width ("1 : 4") 14 00100011	44	2C	Standard timing ID # 4	01	00000001
47 2F Standard timing ID #5 01 00000001 48 30 Standard timing ID #6 01 00000001 59 32 Standard timing ID #7 01 00000001 50 32 Standard timing ID #7 01 00000001 51 33 Standard timing ID #7 01 00000001 52 34 Standard timing ID #8 01 00000001 53 35 Standard timing ID #8 01 00000001 54 36 VESA CVT Rev1.1) 55 37 # 1Pixel clock (hex LSB first) 12 10111100 55 37 # 1Pixel dlock (hex LSB first) 1B 00011011 56 38 #1 H active ("1366") 56 01101010 57 39 #1 H blank ("100") 50 01010000 59 38 #1 V active ("768") 00 00000000 60 3C #1 V blank ("20") 14 00001000 61 3D #1 V active : V blank ("32") 10 00000000 62 3E #1 H sync offset : H sync pulse width ("1:4") 10 0000000000000000000000000000000000	45	2D	Standard timing ID # 4	01	0000001
48 30 Standard timing ID # 6 01 00000001 49 31 Standard timing ID # 6 01 00000001 50 32 Standard timing ID # 7 01 00000001 51 33 Standard timing ID # 7 01 00000001 52 34 Standard timing ID # 8 01 00000001 53 35 Standard timing ID # 8 01 00000001 54 36 VESA CVT Rev1.1) 12 1011110 55 37 # 1 Pixel clock (hex LSB first) 18 00011011 56 38 # 1 H active ("1366") 56 01010110 57 39 # 1 H blank ("100") 64 10000100 58 3A # 1 H active ("1366") 50 01010000 60 3C # 1 V blank ("20") 14 0001000 61 3D # 1 V scrive ("788") 30 00110000 62 3E # 1 H sync offset : V sync pulse width ("1:4") 14 0001010 65 41 H sync offset : H sync pulse width ("1:4") AE 10011010 67 43 # 1 V image size ("174 mm") AE 10110110 68 44 # 1 H image size ("174 mm") AE 10101101 69 45 # 1 H boarder ("0") 00 0000000 70 46 # 1 V boarder ("0") 00 0000000 71 48 # 2 H active ("1366") 100") 100 0000000 72 48 # 2 H blank ("100") 10 00000000 73 49 # 1 Pixel clock (hex LSB first) 11 00000000 74 4A # 2 H active ("1966") 10 00 0000000000000000000000000000000	46	2E	Standard timing ID # 5	01	0000001
49 31 Standard timing ID # 6 01 00000001	47	2F	Standard timing ID # 5	01	00000001
50 32 Standard timing ID # 7 01 00000001 51 33 Standard timing ID # 8 01 00000001 52 34 Standard timing ID # 8 01 00000001 53 35 Standard timing description # 1 Pixel clock ("69.3MHz", According to VESA CVT Rev1.1) 12 10111100 54 36 Detailed timing description # 1 Pixel clock ("69.3MHz", According to VESA CVT Rev1.1) 12 10111100 55 37 # 1 Pixel clock (hex LSB first) 1B 00011011 56 38 # 1 H active ("1366") 56 01010110 57 39 # 1 H blank ("100") 50 01010000 58 3A # 1 H active : H blank ("1366: 100") 50 01010000 59 3B # 1 V active : V blank ("768 :20") 30 00110000 60 3C # 1 H sync offset ("48") 30 00110000 61 3D # 1 H sync offset ("48") 30 00110000 63 3F # 1 H sync offset : V sync offset : V sync offset : V sync width ("1:4")	48	30	Standard timing ID # 6	01	00000001
51 33 Standard timing ID # 7 01 00000001 52 34 Standard timing ID # 8 01 00000001 53 35 Standard timing ID # 8 01 00000001 54 36 VESA CVT Rev1.1) 12 10111100 55 37 # 1 Pixel clock (hex LSB first) 1B 00011011 56 38 # 1 H active ("1366") 56 01010110 57 39 # 1 H blank ("100") 64 10000100 58 3A # 1 H active : H blank ("1366 : 100") 50 01010000 59 3B # 1 V active ("768") 00 0000000 60 3C # 1 V blank ("20") 14 00010110 61 3D # 1 V active : V blank ("768 : 20") 30 00110000 62 3E # 1 H sync offset ("48") 30 00110000 63 3F # 1 H sync offset ("48") 30 00110000 64 40 # 1 V sync offset : V sync pulse width : V sync offset : V sync width ("48	49	31	Standard timing ID # 6	01	0000001
52 34 Standard timing ID # 8 01 00000001 53 35 Standard timing ID # 8 01 00000001 54 36 VESA CVT Rev1.1) 12 10111100 55 37 # 1 Pixel clock (hex LSB first) 1B 00011011 56 38 # 1 H active ("1366") 56 0101010 57 39 # 1 H blank ("100") 64 10000100 58 3A # 1 H active : H blank ("1366 : 100") 50 01010000 69 3C # 1 V blank ("20") 14 00010010 60 3C # 1 V blank ("20") 14 0001010 61 3D # 1 V active : V blank ("768: 20") 30 0011000 62 3E # 1 H sync offset ("48") 30 0011000 63 3F # 1 H sync offset ("48") 30 0011000 64 40 # 1 V sync offset : V sync bulse width ("1 : 4") 14 0001000 64 41 I wise in thin sync pulse width ("3 : 4") <	50	32	Standard timing ID # 7	01	00000001
53 35 Standard timing ID # 8 01 00000001 54 Detailed timing description # 1 Pixel clock ("69.3MHz", According to VESA CVT Rev1.1) 12 10111100 55 37 # 1 Pixel clock (hex LSB first) 1B 00011011 56 38 # 1 H active ("1366") 56 01010110 57 39 # 1 H blank ("100") 64 10000100 58 3A # 1 H active : H blank ("1366 : 100") 50 01010000 59 3B # 1 V active : V blank ("20") 14 00010110 60 3C # 1 V blank ("20") 30 00110000 61 3D # 1 V active : V blank ("768 :20") 30 00110000 62 3E # 1 H sync offset : V sync diffset : V sync buse width ("1 : 4") 20 0010000 63 3F # 1 H sync offset : V sync pulse width ("1 : 4") 14 00011010 65 41 1 H sync offset : V sync pulse width ("1 : 4") 14 0001010 66 42 # 1 H image size ("309 mm") 35 0011010 <td>51</td> <td>33</td> <td>Standard timing ID # 7</td> <td>01</td> <td>0000001</td>	51	33	Standard timing ID # 7	01	0000001
54 36 Detailed timing description # 1 Pixel clock ("69.3MHz", According to VESA CVT Rev1.1) 12 10111100 55 37 # 1 Pixel clock (hex LSB first) 1B 00011011 56 38 # 1 H active ("1366") 56 01010110 57 39 # 1 H blank ("100") 64 10000100 58 3A # 1 H active ("768") 00 00000000 60 3C # 1 V blank ("20") 14 0001010 61 3D # 1 V active : V blank ("768 :20") 30 00110000 62 3E # 1 H sync offset ("48") 30 00110000 63 3F # 1 H sync pulse width ("32") 20 00100000 64 40 # 1 V sync offset : V sync pulse width ("1 : 4") 14 0001100 65 41 ("48:32: 1: 4") 30 00110010 66 42 # 1 H image size ("309 mm") 35 0011011 67 43 # 1 V image size ("174 mm") AE 10101110 68 45	52	34	Standard timing ID # 8	01	0000001
34 36 VESA CVT Rev1.1) 12 1011100 55 37 # 1 Pixel clock (hex LSB first) 1B 00011011 56 38 # 1 H active ("1366") 56 01010110 57 39 # 1 H blank ("100") 64 10000100 58 3A # 1 H active : H blank ("1366 : 100") 50 01010000 59 3B # 1 V active ("768") 00 00000000 60 3C # 1 V blank ("20") 14 00010110 61 3D # 1 V active : V blank ("768:20") 30 00110000 62 3E # 1 H sync offset ("48") 30 00110000 63 3F # 1 H sync offset : V sync pulse width ("1:4") 40 00110000 64 40 # 1 V sync offset : V sync pulse width : V sync offset : V sync width 00 00000000 65 41 ("48:32:1:4") 00 00000000 66 42 # 1 H image size ("309 mm") 35 00110110 67 43 # 1 V image	53	35		01	00000001
56 38 # 1 H active ("1366") 56 01010110 57 39 # 1 H blank ("100") 64 10000100 58 3A # 1 H active : H blank ("1366 : 100") 50 01000000 59 3B # 1 V cative ("768") 00 00000000 60 3C # 1 V blank ("20") 14 00010110 61 3D # 1 V active : V blank ("768 : 20") 30 00110000 62 3E # 1 H sync offset ("48") 30 00110000 63 3F # 1 H sync offset : V sync pulse width ("32") 20 00100000 64 40 # 1 V sync offset : V sync pulse width : V sync offset : V sync width 41 00010100 65 # 1 H sync offset : V sync pulse width : V sync offset : V sync width 41 00010000 66 42 # 1 H image size ("309 mm") 35 0011010 67 43 # 1 V image size ("174 mm") AE 1010111 68 44 # 1 H image size ("309 mm") AE 1010110 67	54	36		12	10111100
57 39 # 1 H blank ("100") 64 10000100 58 3A # 1 H active : H blank ("1366 : 100") 50 01010000 59 3B # 1 V active ("768") 00 00000000 60 3C # 1 V blank ("20") 14 00010110 61 3D # 1 V active : V blank ("768 : 20") 30 00110000 62 3E # 1 H sync offset ("48") 30 00110000 63 3F # 1 H sync offset : V sync pulse width ("1 : 4") 14 0001000 64 40 # 1 V sync offset : V sync pulse width ("1 : 4") 14 0001000 65 # 1 H sync offset : H sync pulse width : V sync offset : V sync width 00 00000000 66 42 # 1 H image size ("309 mm") 35 0011010 67 43 # 1 V image size ("174 mm") AE 10101110 68 44 # 1 H image size ("174 mm") AE 1010110 69 45 # 1 H boarder ("0") 00 00000000 70 46	55	37	# 1 Pixel clock (hex LSB first)	1B	00011011
58 3A # 1 H active : H blank ("1366 : 100") 50 01010000 59 3B # 1 V active ("768") 00 00000000 60 3C # 1 V blank ("20") 14 00010110 61 3D # 1 V blank ("768 : 20") 30 00110000 62 3E # 1 H sync offset ("48") 30 00110000 63 3F # 1 H sync pulse width ("32") 20 00100000 64 40 # 1 V sync offset : V sync pulse width ("1 : 4") 14 0001010 65 41 "1 H sync offset : H sync pulse width : V sync offset : V sync width 00 00000000 65 41 "1 H sync offset : H sync pulse width : V sync offset : V sync width 00 00000000 65 41 H 1 sync offset : H sync pulse width : V sync offset : V sync width 00 00000000 66 42 # 1 H image size : V image size ("309 : 174") 10 00010000 67 43 # 1 V boarder ("0") 00 00000000 70 46 # 1 boarder ("0") 00 <td>56</td> <td>38</td> <td># 1 H active ("1366")</td> <td>56</td> <td>01010110</td>	56	38	# 1 H active ("1366")	56	01010110
59 3B # 1 V active ("768") 00 00000000 60 3C # 1 V blank ("20") 14 00010100 61 3D # 1 V active : V blank ("768 :20") 30 00110000 62 3E # 1 H sync offset ("48") 30 00110000 63 3F # 1 H sync pulse width ("32") 20 00100000 64 40 # 1 V ync offset : V sync pulse width : V sync offset : V sync width 00 00000000 65 # 1 H sync offset : H sync pulse width : V sync offset : V sync width 00 00000000 66 42 # 1 H image size ("309 mm") AE 10101110 67 43 # 1 V image size ("174 mm") AE 10101110 68 44 # 1 H image size : V image size ("309 : 174") 10 0001000 69 45 # 1 H boarder ("0") 00 00000000 70 46 # 1 V boarder ("0") 00 00000000 47 ; H sync POL is positive 1A 00011000 72 Detailed timing descri	57	39	# 1 H blank ("100")	64	10000100
60 3C # 1 V blank ("20") 14 00010110 61 3D # 1 V active : V blank ("768 :20") 30 00110000 62 3E # 1 H sync offset ("48") 30 00110000 63 3F # 1 H sync pulse width ("32") 20 00100000 64 40 # 1 V sync offset : V sync pulse width ("1 : 4") 14 00010100 65 41 H 1 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 1 : 4") 00 00000000 66 42 # 1 H image size ("309 mm") 35 00110101 67 43 # 1 V image size ("174 mm") AE 10101110 68 44 # 1 H image size ("174 mm") AE 10101110 69 45 # 1 H boarder ("0") 00 00000000 70 46 # 1 V boarder ("0") 00 00000000 71 47 H sync POL is positive 1A 00011000 72 48 # 1 H image size ("136") 00 00000000 73 <t< td=""><td>58</td><td>3A</td><td># 1 H active : H blank ("1366 : 100")</td><td>50</td><td>01010000</td></t<>	58	3A	# 1 H active : H blank ("1366 : 100")	50	01010000
61 3D # 1 V active : V blank ("768 :20") 30 00110000 62 3E # 1 H sync offset ("48") 30 00110000 63 3F # 1 H sync pulse width ("32") 20 00100000 64 40 # 1 V sync offset : V sync pulse width ("1 : 4") 14 00010100 65 # 1 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 1 : 4") 00 00000000 66 42 # 1 H image size ("309 mm") 35 00110101 67 43 # 1 V image size ("174 mm") AE 10101110 68 44 # 1 H image size : V image size ("309 : 174") 10 00010000 69 45 # 1 H boarder ("0") 00 00000000 70 46 # 1 V boarder ("0") 00 00000000 71 sync POL is negative ; H sync POL is positive 1A 00011000 72 48 # 1 Pixel clock (hex LSB first) 12 00000000 74 4A # 2 H active ("1366") 56 0000000 75	59	3B	# 1 V active ("768")	00	00000000
62 3E # 1 H sync offset ("48") 30 00110000 63 3F # 1 H sync pulse width ("32") 20 00100000 64 40 # 1 V sync offset : V sync pulse width ("1 : 4") 14 00010100 65 41 ("48: 32 : 1 : 4") 00 00000000 66 42 # 1 H image size ("309 mm") 35 00110101 67 43 # 1 V image size ("174 mm") AE 10101110 68 44 # 1 H image size : V image size ("309 : 174") 10 00010000 69 45 # 1 H boarder ("0") 00 00000000 70 46 # 1 V boarder ("0") 00 00000000 71 48 H sync POL is negative 1A 00011000 72 48 Detailed timing description # 1 Pixel clock ("46.21MHz", According to VESA CVT Rev1.1) 0D 00000000 73 49 # 1 Pixel clock (hex LSB first) 12 00000000 74 4A # 2 H active ("1366") 56 00000000 75	60	3C	# 1 V blank ("20")	14	00010110
63 3F # 1 H sync pulse width ("32") 20 00100000 64 40 # 1 V sync offset : V sync pulse width ("1 : 4") 14 00010100 65 41 # 1 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 1 : 4") 00 00000000 66 42 # 1 H image size ("309 mm") 35 00110101 67 43 # 1 V image size ("174 mm") AE 10101110 68 44 # 1 H image size : V image size ("309 : 174") 10 00010000 69 45 # 1 H boarder ("0") 00 00000000 70 46 # 1 V boarder ("0") 00 00000000 71 sync POL is negative ; H sync POL is positive 1A 00011000 72 48 VESA CVT Rev1.1) 0D 00000000 73 49 # 1 Pixel clock (hex LSB first) 12 00000000 74 4A # 2 H active ("1366") 56 00000000 75 4B # 2 H blank ("100") 50 00000000 76 4C # 2 H active : H blank ("1366 : 100") 50 00000000	61	3D	# 1 V active : V blank ("768 :20")	30	00110000
64 40 # 1 V sync offset : V sync pulse width ("1 : 4") 14 00010100 65 # 1 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 1 : 4") 00 00000000 66 42 # 1 H image size ("309 mm") 35 00110101 67 43 # 1 V image size ("174 mm") AE 10101110 68 44 # 1 H image size : V image size ("309 : 174") 10 00010000 69 45 # 1 H boarder ("0") 00 00000000 70 46 # 1 V boarder ("0") 00 00000000 71 # 1 Non-interlaced ; Normal display, no stereo ; Digital Separate ; V sync POL is negative ; H sync POL is positive 1A 00011000 72 48 VESA CVT Rev1.1) 0D 00000000 73 49 # 1 Pixel clock (hex LSB first) 12 00000000 74 4A # 2 H active ("1366") 56 00000000 75 4B # 2 H blank ("100") 50 00000000 77 4D # 2 V active ("768") 00 01001110	62	3E	# 1 H sync offset ("48")	30	00110000
# 1 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 1 : 4") 66	63	3F		20	00100000
65 # 1 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 1 : 4") 00 00000000 66 42 # 1 H image size ("309 mm") 35 00110101 67 43 # 1 V image size ("174 mm") AE 10101110 68 44 # 1 H image size : V image size ("309 : 174") 10 00010000 69 45 # 1 H boarder ("0") 00 00000000 70 46 # 1 V boarder ("0") 00 00000000 71 # 1 Non-interlaced ; Normal display, no stereo ; Digital Separate ; V sync POL is negative ; H sync POL is positive 1A 00011000 72 48 Detailed timing description # 1 Pixel clock ("46.21MHz", According to VESA CVT Rev1.1) 0D 00000000 73 49 # 1 Pixel clock (hex LSB first) 12 00000000 74 4A # 2 H active ("1366") 56 00000000 75 4B # 2 H blank ("100") 64 11111110 76 4C # 2 H active : H blank ("1366 : 100") 50 00000000 77 4D # 2 V active ("768") 00 01001110 78 4E # 2 V blank ("20") 30 00110001	64	40	# 1 V sync offset : V sync pulse width ("1 : 4")	14	00010100
67 43 # 1 V image size ("174 mm") AE 10101110 68 44 # 1 H image size : V image size ("309 : 174") 10 00010000 69 45 # 1 H boarder ("0") 00 00000000 70 46 # 1 V boarder ("0") 00 00000000 71 # 1 Non-interlaced ; Normal display, no stereo ; Digital Separate ; V sync POL is negative ; H sync POL is positive 1A 00011000 72 48 Detailed timing description # 1 Pixel clock ("46.21MHz", According to VESA CVT Rev1.1) 0D 00000000 73 49 # 1 Pixel clock (hex LSB first) 12 00000000 74 4A # 2 H active ("1366") 56 00000000 75 4B # 2 H blank ("100") 64 11111110 76 4C # 2 H active : H blank ("1366 : 100") 50 00000000 77 4D # 2 V active ("768") 00 01001110 78 4E # 2 V blank ("20") 14 0011000 79 4F # 2 V active : V blank ("768 :20") 30 00110100 80 50 # 2 H sync offset : V sync pulse width	65	41		00	00000000
68 44 # 1 H image size : V image size ("309 : 174") 10 00010000 69 45 # 1 H boarder ("0") 00 00000000 70 46 # 1 V boarder ("0") 00 00000000 71 # 1 Non-interlaced ; Normal display, no stereo ; Digital Separate ; V sync POL is negative ; H sync POL is positive 1A 00011000 72 Detailed timing description # 1 Pixel clock ("46.21MHz", According to VESA CVT Rev1.1) 0D 00000000 73 49 # 1 Pixel clock (hex LSB first) 12 00000000 74 4A # 2 H active ("1366") 56 00000000 75 4B # 2 H blank ("100") 64 11111110 76 4C # 2 H active : H blank ("1366 : 100") 50 00000000 77 4D # 2 V active ("768") 00 01001110 78 4E # 2 V blank ("20") 14 00110001 79 4F # 2 V active : V blank ("768 :20") 30 00110100 80 50 # 2 H sync offset ("48") 30 00110000 81 51 # 2 H sync offset : V sync pulse width ("1 : 4")	66	42	# 1 H image size ("309 mm")	35	00110101
69 45 # 1 H boarder ("0") 00 00000000 70 46 # 1 V boarder ("0") 00 00000000 71 # 1 Non-interlaced; Normal display, no stereo; Digital Separate; V sync POL is negative; H sync POL is positive 1A 00011000 72 48 Detailed timing description # 1 Pixel clock ("46.21MHz", According to VESA CVT Rev1.1) 0D 00000000 73 49 # 1 Pixel clock (hex LSB first) 12 00000000 74 4A # 2 H active ("1366") 56 00000000 75 4B # 2 H blank ("100") 64 11111110 76 4C # 2 H active: H blank ("1366: 100") 50 00000000 77 4D # 2 V active: ("768") 00 01001110 78 4E # 2 V blank ("20") 14 00110001 79 4F # 2 V active: V blank ("768:20") 30 00110100 80 50 # 2 H sync offset ("48") 30 00110000 81 51 # 2 H sync offset: V sync pulse width ("1:4") 14 01000111 82 52 # 2 V sync offset: H sync pulse width: V sync o	67	43	# 1 V image size ("174 mm")	AE	10101110
70 46 # 1 V boarder ("0") 00 000000000 71 # 1 Non-interlaced; Normal display, no stereo; Digital Separate; V sync POL is negative; H sync POL is positive 1A 00011000 72 Detailed timing description # 1 Pixel clock ("46.21MHz", According to VESA CVT Rev1.1) 0D 00000000 73 49 # 1 Pixel clock (hex LSB first) 12 00000000 74 4A # 2 H active ("1366") 56 00000000 75 4B # 2 H blank ("100") 64 11111110 76 4C # 2 H active : H blank ("1366 : 100") 50 00000000 77 4D # 2 V active ("768") 00 01001110 78 4E # 2 V blank ("20") 14 00110001 79 4F # 2 V active : V blank ("768 :20") 30 00110100 80 50 # 2 H sync offset ("48") 30 00110000 81 51 # 2 H sync pulse width ("32") 20 01000010 82 52 # 2 V sync offset : V sync pulse width : V sync offset : V sync width ("48: 32 : 1 : 4") 00 01000101	68	44	# 1 H image size : V image size ("309 : 174")	10	00010000
# 1 Non-interlaced; Normal display, no stereo; Digital Separate; V sync POL is negative ; H sync POL is positive Detailed timing description # 1 Pixel clock ("46.21MHz", According to VESA CVT Rev1.1) # 1 Pixel clock (hex LSB first) 12 00000000 # 2 H active ("1366") # 2 H active: H blank ("100") # 2 V active: H blank ("1366: 100") # 2 V active: W blank ("366: 100") # 2 V active: V blank ("768: 20") # 2 H sync offset: V sync pulse width ("1: 4") # 2 H sync offset: H sync pulse width: V sync offset: V sync width ("48: 32: 1: 4")	69	45	# 1 H boarder ("0")	00	00000000
71 sync POL is negative 1A 00011000 72 Detailed timing description # 1 Pixel clock ("46.21MHz", According to VESA CVT Rev1.1) 0D 00000000 73 49 # 1 Pixel clock (hex LSB first) 12 00000000 74 4A # 2 H active ("1366") 56 00000000 75 4B # 2 H blank ("100") 64 11111110 76 4C # 2 H active : H blank ("1366 : 100") 50 00000000 77 4D # 2 V active ("768") 00 01001110 78 4E # 2 V blank ("20") 14 00110001 79 4F # 2 V active : V blank ("768 :20") 30 00110100 80 50 # 2 H sync offset ("48") 30 00110000 81 51 # 2 H sync pulse width ("32") 20 01000010 82 52 # 2 V sync offset : V sync pulse width : V sync offset : V sync width ("48: 32 : 1 : 4") 00 01000101	70	46	# 1 V boarder ("0")	00	00000000
72 As VESA CVT Rev1.1) Detailed timing description # 1 Pixel clock ("46.21MHz", According to VESA CVT Rev1.1) 0D 00000000 73 49 # 1 Pixel clock (hex LSB first) 12 00000000 74 4A # 2 H active ("1366") 56 00000000 75 4B # 2 H blank ("100") 64 11111110 76 4C # 2 H active : H blank ("1366 : 100") 50 00000000 77 4D # 2 V active ("768") 00 01001110 78 4E # 2 V blank ("20") 14 00110001 79 4F # 2 V active : V blank ("768 :20") 30 00110100 80 50 # 2 H sync offset ("48") 30 00110000 81 51 # 2 H sync pulse width ("32") 20 01000010 82 52 # 2 V sync offset : V sync pulse width : V sync offset : V sync width ("48: 32 : 1 : 4") 00 01000101	71	47	sync POL is negative	1A	00011000
74 4A # 2 H active ("1366") 56 00000000 75 4B # 2 H blank ("100") 64 11111110 76 4C # 2 H active : H blank ("1366 : 100") 50 00000000 77 4D # 2 V active ("768") 00 01001110 78 4E # 2 V blank ("20") 14 00110001 79 4F # 2 V active : V blank ("768 :20") 30 00110100 80 50 # 2 H sync offset ("48") 30 00110000 81 51 # 2 H sync pulse width ("32") 20 01000010 82 52 # 2 V sync offset : V sync pulse width : V sync offset : V sync width ("48: 32 : 1 : 4") 01000101	72		Detailed timing description # 1 Pixel clock ("46.21MHz", According to	0D	00000000
75	73	49	# 1 Pixel clock (hex LSB first)	12	00000000
76	74	4A	# 2 H active ("1366")	56	00000000
77 4D # 2 V active ("768") 00 01001110 78 4E # 2 V blank ("20") 14 00110001 79 4F # 2 V active : V blank ("768 :20") 30 00110100 80 50 # 2 H sync offset ("48") 30 00110000 81 51 # 2 H sync pulse width ("32") 20 01000010 82 52 # 2 V sync offset : V sync pulse width ("1 : 4") 14 01000111 83 # 2 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 1 : 4") 00 01000101	75	4B	# 2 H blank ("100")	64	11111110
78 4E # 2 V blank ("20") 14 00110001 79 4F # 2 V active : V blank ("768 :20") 30 00110100 80 50 # 2 H sync offset ("48") 30 00110000 81 51 # 2 H sync pulse width ("32") 20 01000010 82 52 # 2 V sync offset : V sync pulse width ("1 : 4") 14 01000111 83 # 2 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 1 : 4") 00 01000101	76	4C	# 2 H active : H blank ("1366 : 100")	50	00000000
79 4F # 2 V active : V blank ("768 :20") 30 00110100 80 50 # 2 H sync offset ("48") 30 00110000 81 51 # 2 H sync pulse width ("32") 20 01000010 82 52 # 2 V sync offset : V sync pulse width ("1 : 4") 14 01000111 83 # 2 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 1 : 4") 00 01000101	77	4D	# 2 V active ("768")	00	01001110
80 50 # 2 H sync offset ("48") 30 00110000 81 51 # 2 H sync pulse width ("32") 20 01000010 82 52 # 2 V sync offset : V sync pulse width ("1 : 4") 14 01000111 83 # 2 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 1 : 4") 00 01000101	78	4E	# 2 V blank ("20")	14	00110001
81 51 # 2 H sync pulse width ("32") 20 01000010 82 52 # 2 V sync offset : V sync pulse width ("1 : 4") 14 01000111 83 # 2 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 1 : 4") 00 01000101	79	4F	# 2 V active : V blank ("768 :20")	30	00110100
81 51 # 2 H sync pulse width ("32") 20 01000010 82 52 # 2 V sync offset : V sync pulse width ("1 : 4") 14 01000111 83 # 2 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 1 : 4") 00 01000101	80	50	# 2 H sync offset ("48")	30	00110000
82 52 # 2 V sync offset : V sync pulse width ("1 : 4") 83 # 2 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 1 : 4") 14 01000111 00 01000101	81	51	# 2 H sync pulse width ("32")	20	01000010
83 # 2 H sync offset : H sync pulse width : V sync offset : V sync width 00 01000101	82	52		14	01000111
84 54 # 2 H image size ("309 mm") 35 00101101	83	53	# 2 H sync offset : H sync pulse width : V sync offset : V sync width	00	01000101
	84	54	# 2 H image size ("309 mm")	35	00101101

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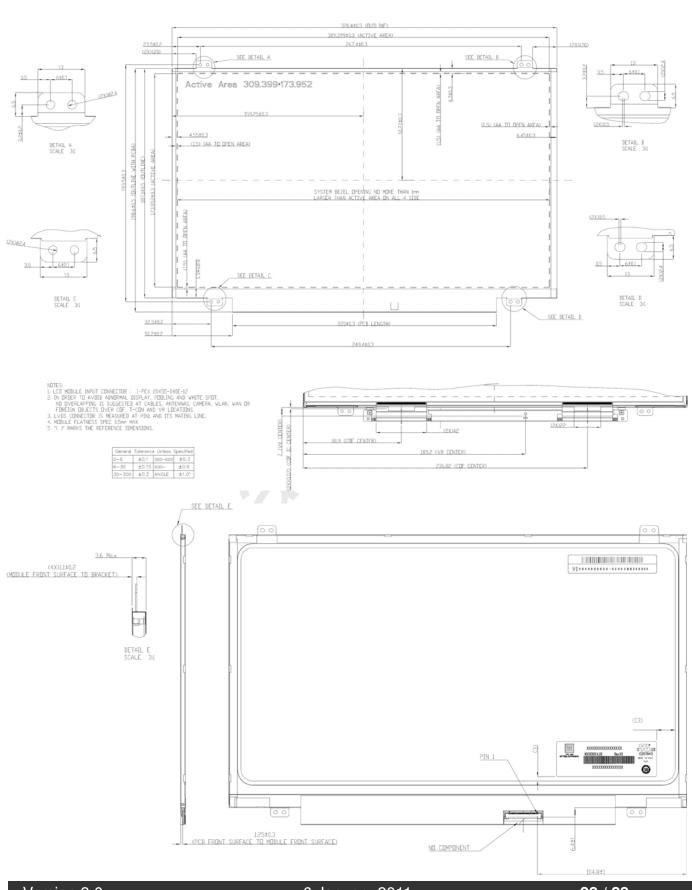
85	55	# 2 V image size ("174 mm")	ΑE	01001100
86	56	# 2 H image size : V image size ("309 : 174")	10	00010000
87	57	# 2 H boarder ("0")	00	00000000
88	58	# 2 V boarder ("0")	00	00000000
89	59	# 2 Non-interlaced; Normal display, no stereo; Digital Separate; V sync POL is negative; H sync POL is positive	1A	00011010
90	5A	NA	00	00000000
91	5B	NA	00	00000000
92	5C	NA	00	00000000
93	5D	NA	00	00000000
94	5E	NA	00	00000000
95	5F	NA	00	00000000
96	60	NA	00	00000000
97	61	NA	00	00000000
98	62	NA	00	00000000
99	63	NA	00	00000000
100	64	NA	00	00000000
101	65	NA	00	00000000
102	66	NA	00	00000000
103	67	NA	00	00000000
104	68	NA	00	00000000
105	69	NA	00	00000000
106	6A	NA	00	00000000
107	6B	NA	00	00000000
108	6C	Detailed Timing Description #4	00	00000000
109	6D	Flags	00	00000000
110	6E	Reserved	00	00000000
111	6F	For Brightness Table and Power Consumption	02	00000010
112	70	Flags	00	00000000
113	71	PWM % [7:0] @ Step 0 = 5 %	0C	00001100
114	72	PWM % [7:0] @ Step 5 = 28 %	47	01000111
115	73	PWM % [7:0] @ Step 10 = 93 %	ED	11101101
116	74	Nits [7:0] @ Step 0 = 11 nits	0A	00001010
117	75	Nits [7:0] @ Step 5 = 60 nits	3C	00111100
118	76	Nits [7:0] @ Step 10 = 200 nits	64	01100100
119	77	Panel Electronics Power @32x32 Chess Pattern = 717 mW	11	00010001
120	78	Backlight Power @60 nits = 746 mW	12	00010010
121	79	Backlight Power @Step 10 = 2423 mW	1E	00011110
122	7A	Nits @ 100% PWM Duty = 215 nits	6B	01101011
123	7B	Flags	00	00000000
124	7C	Flags	00	00000000
125	7D	Flags	00	00000000
126	7E	Extension flag	00	00000000
127	7F	Checksum	DE	11011110

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Appendix. OUTLINE DRAWING



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